Remarks

The Office Action mailed February 18, 2004 has been carefully reviewed and the following remarks have been made in consequence thereof.

Claims 2-5, 7-11, 13-17, 19-22, 24-26, and 28-47 are now pending in this application. Claims 1, 6, 12, 18, 23, and 27 have been canceled without prejudice, waiver, or disclaimer. Claims 2-5, 7-11, 13-17, 19-22, 24-26, 28, 30, and 31 have been amended. No new matter has been added. Claims 2-5, 7-11, 13-17, 19-22, and 24-47 stand rejected.

The rejection of Claims 2-5, 7-11, 13-17, 19-22, and 24-47 under 35 U.S.C. § 112, first paragraph, is respectfully traversed. Applicants have amended Claims 2, 3, 5, 7, 8, 9, 13, 15, 17, 19, 24, 25, 26, and 28. Claims 32 and 33 depend, directly or indirectly, from independent Claim 2, Claims 4, 5, 34, and 35 depend, directly or indirectly, from independent Claim 3, Claims 8-11 and 36-37 depend, directly or indirectly, from independent Claim 7, Claims 14-17 and 38-39 depend, directly or indirectly, from independent Claim 13, Claims 20-22 and 40-41 depend, directly or indirectly, from independent Claim 19, Claims 42 and 43 depend, directly or indirectly, from independent Claim 24, Claims 26 and 44-45 depend, directly or indirectly, from independent Claim 25, and Claims 29-31 and 46-47 depend, directly or indirectly, from independent Claim 28. Accordingly, Applicants respectfully submit that Claims 2-5, 7-11, 13-17, 19-22, and 24-47 particularly point out and distinctly claim the subject matter which the Applicants regard as their invention and request that the rejection of Claims 2-5, 7-11, 13-17, 19-22, and 24-47 under Section 112, first paragraph, be withdrawn.

For the reasons set forth above, Applicants respectfully request that the rejection of Claims 2-5, 7-11, 13-17, 19-22, and 24-47 under Section 112, first paragraph, be withdrawn.

The rejection of Claims 2-5, 7-11, 13-17, 19-22, and 24-47 under 35 U.S.C. § 112, second paragraph, is respectfully traversed. Applicants have amended Claims 2, 3, 4, 7, 10, 11, 13, 14, 16, 19, 20, 22, 24, 25, 28, and 31. Claims 32 and 33 depend, directly or indirectly, from independent Claim 2. Claims 4, 5, 34, and 35 depend, directly or indirectly, from independent Claim 3, Claims 8-11 and 36-37 depend, directly or indirectly, from independent Claim 7, Claims 14-17 and 38-39 depend, directly or indirectly, from independent Claim 13, Claims 20-22 and 40-41 depend, directly or indirectly, from independent Claim 19, Claims

42 and 43 depend, directly or indirectly, from independent Claim 24, Claims 26 and 44-45 depend, directly or indirectly, from independent Claim 25, and Claims 29-31 and 46-47 depend, directly or indirectly, from independent Claim 28. Accordingly, Applicants respectfully request that the rejection of Claims 2-5, 7-11, 13-17, 19-22, and 24-47 under Section 112, second paragraph, be withdrawn.

For the reasons set forth above, Applicants respectfully request that the rejection of Claims 2-5, 7-11, 13-17, 19-22, and 24-47 under Section 112, second paragraph, be withdrawn.

The rejection of Claims 3, 7, 19, and 24 under 35 U.S.C. § 102(b) as being anticipated by Chiriatti (U.S. Patent No. 4,952,934) is respectfully traversed.

Chiriatti describes a device that includes an analog section. The analog section includes a comparator (e.g. a zero-crossing detector) (2), an analog output buffer (1), and a plurality of integrated analog switches (S1, S2, S3 and S4) (column 3, lines 13-18, Figure 1). These analog switches are also driven by a programmable state machine and permit to select a path of analog signals (column 3, lines 18-20). The S1 switch enables the output of an analog signal delivered by a DAC through the output analog buffer and an analog output pin OUT, the switches S2 and S3 permit to feed the same analog signal produced by the DAC and/or an external analog signal applied to an analog input pin IN1, to a first input of the comparator circuit 2, and the switch S4 permits to feed a second external analog signal applied to a second analog input pin (IN2) to the second input of the comparator circuit (column 3, lines 20-31).

Claim 3 recites a control circuit for configuring at least one I/O module connector pin, the circuit comprising "a processor controlling a configuration of the at least one pin via at least one port; a plurality of switch assemblies comprising a plurality of solid state switches, said processor controlling whether a respective solid state switch of said solid state switches is in an open state or a closed state; and a comparator configured to provide an output to said processor, wherein an input of said comparator is coupled to said switch assemblies including said solid state switches and voltage supplies, said switch assemblies configured to operate said at least one pin in one of a plurality of modes."

Chiriatti does not describe or suggest a control circuit as recited in Claim 3. Specifically, Chiriatti does not describe or suggest a comparator, where an input of the comparator is coupled to the switch assemblies including the solid state switches and voltage supplies, and the switch assemblies configured to operate at least one pin in one of a plurality of modes. Rather, Chiriatti describes a comparator having a first input that receives, via a switch S2 an analog signal produced by a DAC and receives via a switch S3 an external analog signal. Accordingly, Chiriatti does not describe or suggest the comparator coupled to the switch assemblies including the voltage supplies. For the reasons set forth above, Claim 3 is submitted to be patentable over Chiriatti.

Claim 7 recites an I/O module comprising "at least one connector pin; a control circuit comprising a plurality of solid state switches, said solid state switches being operated to control a configuration of the at least one pin; and a comparator configured to provide an output to a processor located within said circuit, wherein an input of said comparator is coupled to a plurality of switch assemblies including said solid state switches and voltage supplies, said switch assemblies configured to operate said at least one pin in one of a plurality of modes."

Chiriatti does not describe or suggest an I/O module as recited in Claim 7. Specifically, Chiriatti does not describe or suggest a comparator, where an input of the comparator is coupled to a plurality of switch assemblies including the solid state switches and voltage supplies, the switch assemblies configured to operate at least one pin in one of a plurality of modes. Rather, Chiriatti describes a comparator having a first input that receives, via a switch S2 an analog signal produced by a DAC and receives via a switch S3 an external analog signal. Accordingly, Chiriatti does not describe or suggest a comparator having an input that is coupled to a plurality of switch assemblies including voltage supplies. For the reasons set forth above, Claim 7 is submitted to be patentable over Chiriatti.

Claim 19 recites a method for configuring at least one connector pin utilizing a control circuit, the control circuit including at least one port, the method comprising "providing an energization state to the at least one port; controlling a configuration of the at least one connector pin by utilizing a processor including the at least one port; providing an output from a comparator to the processor located within the control circuit; and coupling an input of the comparator to a plurality of switch assemblies including switches and voltage

supplies, the switch assemblies configured to operate the at least one connector pin in one of a plurality of modes."

Chiriatti does not describe or suggest a method for configuring at least one connector pin as recited in Claim 19. Specifically, Chiriatti does not describe or suggest coupling an input of the comparator to a plurality of switch assemblies including switches and voltage supplies, the switch assemblies configured to operate at least one connector pin in one of a plurality of modes. Rather, Chiriatti describes a comparator having a first input that receives, via a switch S2 an analog signal produced by a DAC and receives via a switch S3 an external analog signal. Accordingly, Chiriatti does not describe or suggest coupling an input of the comparator to a plurality of switch assemblies including voltage supplies. For the reasons set forth above, Claim 19 is submitted to be patentable over Chiriatti.

Claim 24 recites an I/O module comprising "at least one connector pin; a control circuit comprising a processor controlling a configuration of said at least one connector pin by operating a plurality of switches; and a comparator configured to provide an output to said processor located within said circuit, wherein an input of said comparator is coupled to a plurality of switch assemblies including said switches and voltage supplies, said switch assemblies configured to operate said at least one connector pin in one of a plurality of modes."

Chiriatti does not describe or suggest an I/O module as recited in Claim 24. Specifically, Chiriatti does not describe or suggest a comparator, where an input of the comparator is coupled to a plurality of switch assemblies including the switches and voltage supplies, the switch assemblies configured to operate at least one connector pin in one of a plurality of modes. Rather, Chiriatti describes a comparator having a first input that receives, via a switch S2 an analog signal produced by a DAC and receives via a switch S3 an external analog signal. Accordingly, Chiriatti does not describe or suggest a comparator having an input coupled to a plurality of switch assemblies including voltage supplies. For the reasons set forth above, Claim 24 is submitted to be patentable over Chiriatti.

For the reasons set forth above, Applicants respectfully request that the Section 102 rejection of Claims 3, 7, 19, and 24 be withdrawn.

The rejection of Claims 2, 4-5, 8-11, and 20-22 under 35 U.S.C. § 102(b) as being anticipated by Piasecki et al. (U.S. Patent No. 6,509,758) is respectfully traversed.

Applicants respectfully submit that Piasecki et al. is not a prior art reference under 35 U.S.C. § 102(b) because the invention in Piasecki et al. is not patented more than one year prior to the date, July 16, 2001, of the present application for patent in the United States (MPEP 2133). Piaseki was patented on January 21, 2003. Accordingly, Applicants respectfully submit that Piasecki et al. is not a prior art reference under 35 U.S.C. § 102(b). However, Applicants assume that Piasecki et al. is prior art under 35 U.S.C. § 102(e).

Piasecki et al. describe a system in which analog signals coupled to a pin interface (14) can be coupled on a line (62) to a comparator (25) for comparison with either a fixed or programmable reference voltage (column 3, lines 44-49, Figure 1). The pin interface can couple analog signals to analog circuits, such as an analog-to-digital converter (22), by way of a common analog line (32) (column 3, lines 36-38). If all analog lines of each pin interface are to be used for comparison with the reference voltage, the common analog line can be connected to an input of the comparator (column 5, lines 6-10).

Claim 2 recites a control circuit for configuring at least one I/O module connector pin, the circuit comprising "a processor controlling a configuration of the at least one pin via at least one port, wherein one of said at least one port is configured to be one of a Pull-Down (PD) port, a Pull-Up (PU) port, a Discrete High (DH) port, a Discrete Low (DL) port, a positive 15 volt (P15V) port, a negative 15 volt (N15V) port, a range (RANGE) port, and a voltage out (VOUT) port; and a comparator configured to provide an output to a processor located within said circuit, wherein an input of said comparator is coupled to a plurality of switch assemblies including switches and voltage supplies, said switch assemblies configured to operate said at least one pin in one of a plurality of modes."

Piasecki et al. do not describe or suggest a control circuit as recited in Claim 2. Specifically, Piasecki et al. do not describe or suggest a comparator, where an input of the comparator is coupled to a plurality of switch assemblies including switches and voltage supplies, the switch assemblies configured to operate at least one pin in one of a plurality of modes. Rather, Piasecki et al. describe a comparator that receives analog signals from a pin interface and an input of the comparator that is coupled to a common analog line that is further coupled to an analog to digital converter. Accordingly, Piasecki et al. does not

describe or suggest the comparator coupled to a plurality of switch assemblies including voltage supplies. For the reasons set forth above, Claim 2 is submitted to be patentable over Piasecki et al.

Claims 4-5 depend on independent Claim 3 which recites a control circuit for configuring at least one I/O module connector pin, the circuit comprising "a processor controlling a configuration of the at least one pin via at least one port; a plurality of switch assemblies comprising a plurality of solid state switches, said processor controlling whether a respective solid state switch of said solid state switches is in an open state or a closed state; and a comparator configured to provide an output to said processor, wherein an input of said comparator is coupled to said switch assemblies including said solid state switches and voltage supplies, said switch assemblies configured to operate said at least one pin in one of a plurality of modes."

Piasecki et al. does not describe or suggest a control circuit as recited in Claim 3. Specifically, Piasecki et al. does not describe or suggest a comparator, where an input of the comparator is coupled to the switch assemblies including the solid state switches and voltage supplies, and the switch assemblies configured to operate at least one pin in one of a plurality of modes. Rather, Piasecki et al. describe a comparator that receives analog signals from a pin interface and an input of the comparator that is coupled to a common analog line that is further coupled to an analog to digital converter. Accordingly, Piasecki et al. does not describe or suggest the comparator coupled to the switch assemblies including voltage supplies. For the reasons set forth above, Claim 3 is submitted to be patentable over Piasecki et al.

When the recitations of Claims 4 and 5 are considered in combination with the recitations of Claim 3, Applicants submit that dependent Claims 4 and 5 likewise are patentable over Piasecki et al.

Claims 8-11 depend, directly or indirectly, from independent Claim 7 which recites an I/O module comprising "at least one connector pin; a control circuit comprising a plurality of solid state switches, said solid state switches being operated to control a configuration of the at least one pin; and a comparator configured to provide an output to a processor located within said circuit, wherein an input of said comparator is coupled to a plurality of switch

assemblies including said solid state switches and voltage supplies, said switch assemblies configured to operate said at least one pin in one of a plurality of modes."

Piasecki et al. does not describe or suggest an I/O module as recited in Claim 7. Specifically, Piasecki et al. does not describe or suggest a comparator, where an input of the comparator is coupled to a plurality of switch assemblies including the solid state switches and voltage supplies, the switch assemblies configured to operate at least one pin in one of a plurality of modes. Rather, Piasecki et al. describe a comparator that receives analog signals from a pin interface and an input of the comparator coupled to a common analog line coupled to an analog to digital converter. Accordingly, Piasecki et al. does not describe or suggest a comparator having an input that is coupled to a plurality of switch assemblies including voltage supplies. For the reasons set forth above, Claim 7 is submitted to be patentable over Piasecki et al.

When the recitations of Claims 8-11 are considered in combination with the recitations of Claim 7, Applicants submit that dependent Claims 8-11 likewise are patentable over Piasecki et al.

Claims 20-22 depend, directly or indirectly, from independent Claim 19 which recites a method for configuring at least one connector pin utilizing a control circuit, the control circuit including at least one port, the method comprising "providing an energization state to the at least one port; controlling a configuration of the at least one connector pin by utilizing a processor including the at least one port; providing an output from a comparator to the processor located within the control circuit; and coupling an input of the comparator to a plurality of switch assemblies including switches and voltage supplies, the switch assemblies configured to operate the at least one connector pin in one of a plurality of modes."

Piasecki et al. does not describe or suggest a method for configuring at least one connector pin as recited in Claim 19. Specifically, Piasecki et al. does not describe or suggest coupling an input of the comparator to a plurality of switch assemblies including switches and voltage supplies, the switch assemblies configured to operate at least one connector pin in one of a plurality of modes. Rather, Piasecki et al. describe a comparator that receives analog signals from a pin interface and an input of the comparator that is coupled to a common analog line that is further coupled to an analog to digital converter. Accordingly, Piasecki et al. does not describe or suggest coupling an input of the comparator to a plurality

of switch assemblies including voltage supplies. For the reasons set forth above, Claim 19 is submitted to be patentable over Piasecki et al.

When the recitations of Claims 20-22 are considered in combination with the recitations of Claim 19, Applicants submit that dependent Claims 20-22 likewise are patentable over Piasecki et al.

For the reasons set forth above, Applicants respectfully request that the Section 102 rejection of Claims 2, 4-5, 8-11, and 20-22 be withdrawn.

The rejection of Claims 13-17, 25-27, 28-31, and 32-47 under 35 U.S.C. § 103(a) as being unpatentable over Piasecki et al. in view of Applicants' admitted prior art is respectfully traversed.

Applicant respectfully traverses any suggestion in paragraph 12 of the Office Action that paragraph 20 is Applicants' admitted prior art. Applicants respectfully submit that paragraph 20 describes "a circuit 110 that is configurable such that pin 112 can be used in various modes", and describes the various modes. Applicants respectfully submit that the various modes implemented by circuit 110 are not prior art.

Piasecki et al. is described above. Applicants' admitted prior art describes input/output (I/O) modules that are utilized to connect a device, such as a programmable logic controller (PLC) to a machine interface such that the PLC can control a machine (paragraph 2)

Claim 13 recites a PLC comprising "an I/O module comprising at least one connector pin and a control circuit comprising a plurality of ports, a configuration of the at least one connector pin determined by a processor including said ports; a comparator configured to provide an output to said processor located within said circuit, wherein an input of said comparator is coupled to a plurality of switch assemblies including switches and voltage supplies, said switch assemblies configured to operate said at least one connector pin in one of a plurality of modes; and a CPU coupled to said I/O module."

Neither Piasecki et al. nor Applicants' admitted prior art, considered alone or in combination, describe or suggest a PLC as recited in Claim 13. Specifically, neither Piasecki et al. nor Applicants' admitted prior art, considered alone or in combination, describe or

suggest a comparator, where an input of the comparator is coupled to a plurality of switch assemblies including switches and voltage supplies, the switch assemblies configured to operate at least one connector pin in one of a plurality of modes. Rather, Piasecki et al. describe a comparator that receives analog signals from a pin interface and an input of the comparator that is coupled to a common analog line that is further coupled to an analog to digital converter. Applicants' admitted prior art describes input/output modules that are utilized to connect a programmable logic controller to a machine interface. Accordingly, neither Piasecki et al. nor Applicants' admitted prior art, considered alone or in combination, describe or suggest a comparator having an input that is coupled to a plurality of switch assemblies including voltage supplies. For the reasons set forth above, Claim 13 is submitted to be patentable over Piasecki et al. in view of Applicants' admitted prior art.

Claims 14-17 and 38-39 depend, directly or indirectly, from independent Claim 13. When the recitations of Claims 14-17 and 38-39 are considered in combination with the recitations of Claim 13, Applicants submit that dependent Claims 14-17 and 38-39 likewise are patentable over Piasecki et al. in view of Applicants' admitted prior art.

Claim 25 recites an I/O module comprising "at least one connector pin; a control circuit comprising a processor that operates a plurality of switches to control a configuration of said at least one pin, wherein the configuration is one of a twenty-four volt positive logic discrete input mode, a twenty-four volt negative logic discrete input mode, a twenty-four volt high side discrete output mode without open wire detection, a twenty-four volt high side discrete output mode with open wire detection, zero volt low side discrete output mode without open wire detection, a zero volt low side discrete output mode with open wire detection, zero to ten volt analog input mode, and a zero to ten volt analog output mode; and a comparator configured to provide an output to said processor, wherein a first input of said comparator is coupled to a plurality of switch assemblies including said switches and voltage supplies, a second input of said comparator coupled to a digital to analog converter that receives a reference signal from said processor, said switch assemblies configured to operate said at least one connector pin in one of a plurality of modes."

Neither Piasecki et al. nor Applicants' admitted prior art, considered alone or in combination, describe or suggest an I/O module as recited in Claim 25. Specifically, neither Piasecki et al. nor Applicants' admitted prior art, considered alone or in combination, describe or suggest a comparator, where a first input of the comparator is coupled to a

plurality of switch assemblies including the switches and voltage supplies, the switch assemblies configured to operate at least one connector pin in one of a plurality of modes. Rather, Piasecki et al. describe a comparator that receives analog signals from a pin interface and an input of the comparator that is coupled to a common analog line that is further coupled to an analog to digital converter. Applicants' admitted prior art describes input/output modules that are utilized to connect a programmable logic controller to a machine interface. Accordingly, neither Piasecki et al. nor Applicants' admitted prior art, considered alone or in combination, describe or suggest a comparator having a first input that is coupled to a plurality of switch assemblies including voltage supplies. For the reasons set forth above, Claim 25 is submitted to be patentable over Piasecki et al. in view of Applicants' admitted prior art.

Claim 27 has been canceled. Claims 26 and 44-45 depend, directly or indirectly, from independent Claim 25. When the recitations of Claims 26 and 44-45 are considered in combination with the recitations of Claim 25, Applicants submit that dependent Claims 26 and 44-45 likewise are patentable over Piasecki et al. in view of Applicants' admitted prior art.

Claim 28 recites a method for configuring at least one connector pin utilizing a control circuit, the method comprising "controlling a configuration of the at least one connector pin, wherein the configuration is one of a twenty-four volt positive logic discrete input mode, a twenty-four volt negative logic discrete input mode, a twenty-four volt high side discrete output mode without open wire detection, a twenty-four volt high side discrete output mode with open wire detection, a zero volt low side discrete output mode without open wire detection, a zero volt low side discrete output mode with open wire detection, a zero to ten volt analog input mode, and a zero to ten volt analog output mode; providing an output from a comparator to a processor located within the control circuit; coupling a first input of the comparator to a plurality of switch assemblies including a plurality of switches and voltage supplies, the switch assemblies configured to operate the at least one connector pin in one of a plurality of modes; and coupling a second input of the comparator to a digital to analog converter that receives a reference signal from the processor."

Neither Piasecki et al. nor Applicants' admitted prior art, considered alone or in combination, describe or suggest a method for configuring at least one connector pin as recited in Claim 28. Specifically, neither Piasecki et al. nor Applicants' admitted prior art,

considered alone or in combination, describe or suggest coupling a first input of the comparator to a plurality of switch assemblies including a plurality of switches and voltage supplies, the switch assemblies configured to operate at least one connector pin in one of a plurality of modes. Rather, Piasecki et al. describe a comparator that receives analog signals from a pin interface and an input of the comparator that is coupled to a common analog line that is further coupled to an analog to digital converter. Applicants' admitted prior art describes input/output modules that are utilized to connect a programmable logic controller to a machine interface. Accordingly, neither Piasecki et al. nor Applicants' admitted prior art, considered alone or in combination, describe or suggest coupling a first input of the comparator to a plurality of switch assemblies including voltage supplies. For the reasons set forth above, Claim 28 is submitted to be patentable over Piasecki et al. in view of Applicants' admitted prior art.

Claims 29-31 and 46-47 depend, directly or indirectly, from independent Claim 28. When the recitations of Claims 29-31 and 46-47 are considered in combination with the recitations of Claim 25, Applicants submit that dependent Claims 29-31 and 46-47 likewise are patentable over Piasecki et al. in view of Applicants' admitted prior art.

Claims 32 and 33 depend, directly or indirectly, from independent Claim 2 which recites a control circuit for configuring at least one I/O module connector pin, the circuit comprising "a processor controlling a configuration of the at least one pin via at least one port, wherein one of said at least one port is configured to be one of a Pull-Down (PD) port, a Pull-Up (PU) port, a Discrete High (DH) port, a Discrete Low (DL) port, a positive 15 volt (P15V) port, a negative 15 volt (N15V) port, a range (RANGE) port, and a voltage out (VOUT) port; and a comparator configured to provide an output to a processor located within said circuit, wherein an input of said comparator is coupled to a plurality of switch assemblies including switches and voltage supplies, said switch assemblies configured to operate said at least one pin in one of a plurality of modes."

Neither Piasecki et al. nor Applicants' admitted prior art, considered alone or in combination, describe or suggest a control circuit as recited in Claim 2. Specifically, neither Piasecki et al. nor Applicants' admitted prior art, considered alone or in combination, describe or suggest a comparator, where an input of the comparator is coupled to a plurality of switch assemblies including switches and voltage supplies, the switch assemblies configured to operate at least one pin in one of a plurality of modes. Rather, Piasecki et al.

describe a comparator that receives analog signals from a pin interface and an input of the comparator that is coupled to a common analog line that is further coupled to an analog to digital converter. Applicants' admitted prior art describes input/output modules that are utilized to connect a programmable logic controller to a machine interface. Accordingly, neither Piasecki et al. nor Applicants' admitted prior art, considered alone or in combination, describe or suggest the comparator coupled to a plurality of switch assemblies including voltage supplies. For the reasons set forth above, Claim 2 is submitted to be patentable over Piasecki et al. in view of Applicants' admitted prior art.

When the recitations of Claims 32 and 33 are considered in combination with the recitations of Claim 2, Applicants submit that dependent Claims 32 and 33 likewise are patentable over Piasecki et al. in view of Applicants' admitted prior art.

Claims 34 and 35 depend, directly or indirectly, from independent Claim 3 which recites a control circuit for configuring at least one I/O module connector pin, the circuit comprising "a processor controlling a configuration of the at least one pin via at least one port; a plurality of switch assemblies comprising a plurality of solid state switches, said processor controlling whether a respective solid state switch of said solid state switches is in an open state or a closed state; and a comparator configured to provide an output to said processor, wherein an input of said comparator is coupled to said switch assemblies including said solid state switches and voltage supplies, said switch assemblies configured to operate said at least one pin in one of a plurality of modes."

Neither Piasecki et al. nor Applicants' admitted prior art, considered alone or in combination, describe or suggest a control circuit as recited in Claim 3. Specifically, neither Piasecki et al. nor Applicants' admitted prior art, considered alone or in combination, describe or suggest a comparator, where an input of the comparator is coupled to the switch assemblies including the solid state switches and voltage supplies, and the switch assemblies configured to operate at least one pin in one of a plurality of modes. Rather, Piasecki et al. describe a comparator that receives analog signals from a pin interface and an input of the comparator that is coupled to a common analog line that is further coupled to an analog to digital converter. Applicants' admitted prior art describes input/output modules that are utilized to connect a programmable logic controller to a machine interface. Accordingly, neither Piasecki et al. nor Applicants' admitted prior art, considered alone or in combination, describe or suggest the comparator coupled to the switch assemblies including voltage

supplies. For the reasons set forth above, Claim 3 is submitted to be patentable over Piasecki et al. in view of Applicants' admitted prior art.

When the recitations of Claims 34 and 35 are considered in combination with the recitations of Claim 3, Applicants submit that dependent Claims 34 and 35 likewise are patentable over Piasecki et al. in view of Applicants' admitted prior art.

Claims 36 and 37 depend, directly or indirectly, from independent Claim 7 which recites an I/O module comprising "at least one connector pin; a control circuit comprising a plurality of solid state switches, said solid state switches being operated to control a configuration of the at least one pin; and a comparator configured to provide an output to a processor located within said circuit, wherein an input of said comparator is coupled to a plurality of switch assemblies including said solid state switches and voltage supplies, said switch assemblies configured to operate said at least one pin in one of a plurality of modes."

Neither Piasecki et al. nor Applicants' admitted prior art, considered alone or in combination, describe or suggest an I/O module as recited in Claim 7. Specifically, neither Piasecki et al. nor Applicants' admitted prior art, considered alone or in combination, describe or suggest a comparator, where an input of the comparator is coupled to a plurality of switch assemblies including the solid state switches and voltage supplies, the switch assemblies configured to operate at least one pin in one of a plurality of modes. Rather, Piasecki et al. describe a comparator that receives analog signals from a pin interface and an input of the comparator that is coupled to a common analog line that is further coupled to an analog to digital converter. Applicants' admitted prior art describes input/output modules that are utilized to connect a programmable logic controller to a machine interface. Accordingly, neither Piasecki et al. nor Applicants' admitted prior art, considered alone or in combination, describe or suggest a comparator having an input that is coupled to a plurality of switch assemblies including voltage supplies. For the reasons set forth above, Claim 7 is submitted to be patentable over Piasecki et al. in view of Applicants' admitted prior art.

When the recitations of Claims 36 and 37 are considered in combination with the recitations of Claim 7, Applicants submit that dependent Claims 36 and 37 likewise are patentable over Piasecki et al. in view of Applicants' admitted prior art.

Claims 40 and 41 depend, directly or indirectly, from independent Claim 19 which recites a method for configuring at least one connector pin utilizing a control circuit, the control circuit including at least one port, the method comprising "providing an energization state to the at least one port; controlling a configuration of the at least one connector pin by utilizing a processor including the at least one port; providing an output from a comparator to the processor located within the control circuit; and coupling an input of the comparator to a plurality of switch assemblies including switches and voltage supplies, the switch assemblies configured to operate the at least one connector pin in one of a plurality of modes."

Neither Piasecki et al. nor Applicants' admitted prior art, considered alone or in combination, describe or suggest a method for configuring at least one connector pin as recited in Claim 19. Specifically, neither Piasecki et al. nor Applicants' admitted prior art, considered alone or in combination, describe or suggest coupling an input of the comparator to a plurality of switch assemblies including switches and voltage supplies, the switch assemblies configured to operate at least one connector pin in one of a plurality of modes. Rather, Piasecki et al. describe a comparator that receives analog signals from a pin interface and an input of the comparator that is coupled to a common analog line that is further coupled to an analog to digital converter. Applicants' admitted prior art describes input/output modules that are utilized to connect a programmable logic controller to a machine interface. Accordingly, neither Piasecki et al. nor Applicants' admitted prior art, considered alone or in combination, describe or suggest coupling an input of the comparator to a plurality of switch assemblies including voltage supplies. For the reasons set forth above, Claim 19 is submitted to be patentable over Piasecki et al. in view of Applicants' admitted prior art.

When the recitations of Claims 40 and 41 are considered in combination with the recitations of Claim 19, Applicants submit that dependent Claims 40 and 41 likewise are patentable over Piasecki et al. in view of Applicants' admitted prior art.

Claims 42 and 43 depend, directly or indirectly, from independent Claim 24 which recites an I/O module comprising "at least one connector pin; a control circuit comprising a processor controlling a configuration of said at least one connector pin by operating a plurality of switches; and a comparator configured to provide an output to said processor located within said circuit, wherein an input of said comparator is coupled to a plurality of switch assemblies including said switches and voltage supplies, said switch assemblies configured to operate said at least one connector pin in one of a plurality of modes."

Neither Piasecki et al. nor Applicants' admitted prior art, considered alone or in combination, describe or suggest an I/O module as recited in Claim 24. Specifically, neither Piasecki et al. nor Applicants' admitted prior art, considered alone or in combination, describe or suggest a comparator, where an input of the comparator is coupled to a plurality of switch assemblies including the switches and voltage supplies, the switch assemblies configured to operate at least one connector pin in one of a plurality of modes. Rather, Piasecki et al. describe a comparator that receives analog signals from a pin interface and an input of the comparator that is coupled to a common analog line that is further coupled to an analog to digital converter. Applicants' admitted prior art describes input/output modules that are utilized to connect a programmable logic controller to a machine interface. Accordingly, neither Piasecki et al. nor Applicants' admitted prior art, considered alone or in combination, describe or suggest a comparator having an input coupled to a plurality of switch assemblies including voltage supplies. For the reasons set forth above, Claim 24 is submitted to be patentable over Piasecki et al. in view of Applicants' admitted prior art.

When the recitations of Claims 42 and 43 are considered in combination with the recitations of Claim 24, Applicants submit that dependent Claims 42 and 43 likewise are patentable over Piasecki et al. in view of Applicants' admitted prior art.

For at least the reasons set forth above, Applicants respectfully request that the Section 103 rejection of Claims 13-17, 25-27, 28-31, and 32-47 be withdrawn.

Moreover, Applicants respectfully submit that the Section 103 rejections of Claims 13-17, 25-27, 28-31, and 32-47 is not a proper rejection. As is well established, obviousness cannot be established by combining the teachings of the cited art to produce the claimed invention, absent some teaching, suggestion, or incentive supporting the combination. Neither Piasecki et al. nor Applicants' admitted prior art, considered alone or in combination, describe or suggest the claimed combination. Furthermore, in contrast to the assertion within the Office Action, Applicants respectfully submit that it would not be obvious to one skilled in the art to combine Piasecki et al. with Applicants' admitted prior art because there is no motivation to combine the references suggested in the cited art itself.

As the Federal Circuit has recognized, obviousness is not established merely by combining references having different individual elements of pending claims. Ex parte Levengood, 28 U.S.P.Q.2d 1300 (Bd. Pat. App. & Inter. 1993). MPEP 2143.01. Rather,

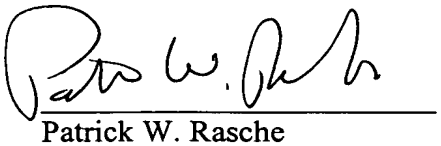
there must be some suggestion, outside of Applicants' disclosure, in the prior art to combine such references, and a reasonable expectation of success must be both found in the prior art, and not based on Applicants' disclosure. In re Vaeck, 20 U.S.P.Q.2d 1436 (Fed. Cir. 1991). In the present case, neither a suggestion or motivation to combine the prior art disclosures, nor any reasonable expectation of success has been shown.

Furthermore, it is impermissible to use the claimed invention as an instruction manual or "template" to piece together the teachings of the cited art so that the claimed invention is rendered obvious. Specifically, one cannot use hindsight reconstruction to pick and choose among isolated disclosures in the art to deprecate the claimed invention. Further, it is impermissible to pick and choose from any one reference only so much of it as will support a given position, to the exclusion of other parts necessary to the full appreciation of what such reference fairly suggests to one of ordinary skill in the art. The present Section 103 rejection is based on a combination of teachings selected from multiple patents in an attempt to arrive at the claimed invention. Specifically, Piasecki et al. teach a comparator that receives analog signals from a pin interface and an input of the comparator that is coupled to a common analog line that is further coupled to an analog to digital converter. Applicants' admitted prior art teaches input/output modules that are utilized to connect a programmable logic controller to a machine interface. Since there is no teaching nor suggestion in the cited art for the combination, the Section 103 rejection appears to be based on a hindsight reconstruction in which isolated disclosures have been picked and chosen in an attempt to deprecate the present invention. Of course, such a combination is impermissible, and for this reason alone, Applicants request that the Section 103 rejections of Claims 13-17, 25-27, 28-31, and 32-47 be withdrawn.

For at least the reasons set forth above, Applicants respectfully request that the rejections of Claims 13-17, 25-27, 28-31, and 32-47 under 35 U.S.C. 103(a) be withdrawn.

In view of the foregoing amendments and remarks, all the claims now active in this application are believed to be in condition for allowance. Reconsideration and favorable action is respectfully solicited.

Respectfully Submitted,



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